

Per-Die Live PDK

Live silicon characterization/model-store/VF constraint deliverable

IP-2012 · Executed digital evidence · RTL / reference evaluation

Function and architecture

- RTL exists
- 82 simulation checks with 0 errors
- BMC + induction proved
- Yosys top garmo_live_pdk reported at 54,040 generic cells. Cross-link Kaldone-Garmo Grain without replacing it

Integration summary

Per-Die Live PDK provides the documented live silicon characterization/model-store/vf constraint deliverable responsibility: Live silicon characterization/model-store/VF constraint deliverable Evaluate the exact IP-2012 implementation and confirm its integration contract before using it inside the target design.

Technical record

Canonical identity	IP-2012
Native implementation identity	IP-2012
Documented responsibility	Live silicon characterization/model-store/VF constraint deliverable
Recorded evidence class	Executed digital evidence
Interface and physical parameters	Bound to the selected source/configuration; not inferred from name or family.

Delivery and release binding

- Exact implementation and configuration manifest
- Documented interfaces and clock/reset contract
- Available reference or verification collateral
- Recorded physical views where authorized and applicable
- Integration acceptance criteria and unresolved gate list

Confirm for the selected release: Source/configuration identity, Interface and dependencies, Verification evidence, Process/library where applicable, Authorized package and acceptance criteria.

Evidence and qualification

RTL exists; 82 simulation checks with 0 errors; BMC + induction proved; Yosys top garmo_live_pdk reported at 54,040 generic cells. Cross-link Kaldone-Garmo Grain without replacing it.

Evidence shown is the Bible record for this canonical implementation, not a fresh tool rerun. External foundry acceptance, silicon measurements, standards certification and unlisted interface/physical parameters are not inferred. Exact delivery and rights are agreed before licensing.

Canonical status: RTL + SIMULATION + FORMAL INDUCTION + GENERIC SYNTHESIS EVIDENCED — no physical implementation or silicon evidence.

Source basis: Bible v7.42 VERIFIED V29, IP-2012; 68.1 Standalone synthesized IP (table 723, row 2).

Evaluation and licensing

Evaluation: Review the exact recorded implementation and agreed test scope. Production: Named-design rights for the agreed qualified release. Custom work: Target integration, verification or physical qualification. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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