COMPUTE & AI

Garmo-RV64-AC

CPU — application-class RISC-V core

IP-2072 · Evaluation package · Evaluation / IP scope

Function and architecture

- RVA23-class baseline, hypervisor, vector and vector-crypto extensions
- 6-wide decode/rename, 10-issue backend, 320-entry ROB, 192-entry load/store queue
- 64 KiB I + 64 KiB D L1
- private 1–2 MiB L2 option

Integration summary

Garmo-RV64-AC integration role: CPU — application-class RISC-V core. Documented composition: RVA23-class baseline, hypervisor, vector and vector-crypto extensions; 6-wide decode/rename, 10-issue backend, 320-entry ROB, 192-entry load/store queue; 64 KiB I + 64 KiB D L1; private 1–2 MiB L2 option.

Technical record

Canonical identity	IP-2072
Responsibility	CPU — application-class RISC-V core
Documented interface architecture	Coherent cache interface, AXI/CHI bridge, AIA, IOMMU hooks, debug/trace
Documented building blocks	RVA23-class baseline, hypervisor, vector and vector-crypto extensions; 6-wide decode/rename, 10-issue backend, 320-entry ROB, 192-entry load/store queue; 64 KiB I + 64 KiB D L1; private 1–2 MiB L2 option
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	6-wide OoO, 320-entry ROB, 2x256-bit RVV, >19.5 SPECint2006/GHz architectural target.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P0 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes.

Source basis: Bible v7.42 IP-2072

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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