MEMORY & STORAGE

Garmo-CXL-2.0

Coherent fabric-memory controller architecture with an explicit protocol and physical-interface boundary.

IP-2077 · Evaluation package · Evaluation / IP scope

Function and architecture

- CXL.io, CXL.cache and CXL.mem with Type 1/2/3 personalities
- CXL 4.0 bundled-port abstraction and memory RAS enhancements
- HDM decoder, poison, patrol scrub, hot-page monitoring and migration assist

Integration summary

Garmo-CXL-2.0 integration role: High-Speed I/O — CXL 4.0 coherent fabric controller. Documented composition: CXL.io, CXL.cache and CXL.mem with Type 1/2/3 personalities; CXL 4.0 bundled-port abstraction and memory RAS enhancements; HDM decoder, poison, patrol scrub, hot-page monitoring and migration assist.

Technical record

Canonical identity	IP-2077
Responsibility	High-Speed I/O — CXL 4.0 coherent fabric controller
Documented interface architecture	PCIe 7 link layer boundary, coherent host/device fabric, memory media interface, FM management
Documented building blocks	CXL.io, CXL.cache and CXL.mem with Type 1/2/3 personalities; CXL 4.0 bundled-port abstraction and memory RAS enhancements; HDM decoder, poison, patrol scrub, hot-page monitoring and migration assist
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	128 GT/s physical generation; Type 1/2/3; bundled ports; low-latency cache/memory paths.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P0 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes.

Source basis: Bible v7.42 IP-2077

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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