FABRIC & CONNECTIVITY

Garmo-UCIe-D2D

Die-to-die controller architecture for chiplet integration; PHY and standards qualification are release-specific.

IP-2078 · Evaluation package · Evaluation / IP scope

Function and architecture

- UCIe 3.0 48/64 GT/s modes with backward compatibility
- Continuous Raw Mode mappings and low-latency streaming
- Management Transport Protocol early firmware download

Integration summary

Garmo-UCIe-D2D integration role: Chiplet I/O — UCIe 3.0 die-to-die controller. Documented composition: UCIe 3.0 48/64 GT/s modes with backward compatibility; Continuous Raw Mode mappings and low-latency streaming; Management Transport Protocol early firmware download.

Technical record

Canonical identity	IP-2078
Responsibility	Chiplet I/O — UCIe 3.0 die-to-die controller
Documented interface architecture	Raw streaming, PCIe/CXL protocol adapter, die-sideband, D2D PHY boundary
Documented building blocks	UCIe 3.0 48/64 GT/s modes with backward compatibility; Continuous Raw Mode mappings and low-latency streaming; Management Transport Protocol early firmware download
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	16–64 GT/s per lane, Standard/Advanced/3D packages, scalable 16/32/64+ lane modules.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

Control/model IP does not establish analog PHY, electrical, RF or standards compliance. Qualified third-party or foundry collateral may be required.

Canonical status: P2 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes. Electrical/PHY production claims require a characterized foundry/node hard-macro backend plus package/channel and compliance evidence.

Source basis: Bible v7.42 IP-2078

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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