INTERFACES & MIXED-SIGNAL

Garmo-SerDes-28G

Adaptive serializer/deserializer control architecture; electrical rate and signal-integrity qualification are separate.

IP-2093 · Evaluation package · Evaluation / IP scope

Function and architecture

- TX FFE, RX CTLE/FFE/DFE with adaptive DSP and continuous calibration
- ADC-based PAM4 receiver with programmable equalizer tap budget
- Digital CDR, baud-rate adaptation and multi-protocol gearbox

Integration summary

Garmo-SerDes-28G integration role: High-Speed I/O — 224 Gb/s-class adaptive SerDes. Documented composition: TX FFE, RX CTLE/FFE/DFE with adaptive DSP and continuous calibration; ADC-based PAM4 receiver with programmable equalizer tap budget; Digital CDR, baud-rate adaptation and multi-protocol gearbox.

Technical record

Canonical identity	IP-2093
Responsibility	High-Speed I/O — 224 Gb/s-class adaptive SerDes
Documented interface architecture	ADC/AFE/DAC hard-macro boundaries, PCS gearbox, FEC metrics, CSR, test pattern
Documented building blocks	TX FFE, RX CTLE/FFE/DFE with adaptive DSP and continuous calibration; ADC-based PAM4 receiver with programmable equalizer tap budget; Digital CDR, baud-rate adaptation and multi-protocol gearbox
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	1–224 Gb/s/lane, NRZ/PAM4, 112 GBd PAM4; >50 dB channel-loss adaptation target; <4 pJ/bit PHY power target on leading node.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

Control/model IP does not establish analog PHY, electrical, RF or standards compliance. Qualified third-party or foundry collateral may be required.

Canonical status: P2 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes. Electrical/PHY production claims require a characterized foundry/node hard-macro backend plus package/channel and compliance evidence.

Source basis: Bible v7.42 IP-2093

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

Contact: patrick@garmolabs.com | Product path: /ip/garmo-serdes-28g