MEMORY & STORAGE

KENBE-DDR

Controller/scheduler above licensed DDR5/MRDIMM-class PHY with QoS, telemetry and fault containment.

IP-3992 · RTL + models · Soft IP / model

Function and architecture

• Controller/scheduler above licensed DDR5/MRDIMM-class PHY with QoS

• telemetry and fault containment

Integration summary

KENBE-DDR addresses controller/scheduler above licensed DDR5/MRDIMM-class PHY with QoS, telemetry and fault containment.

Technical record

Canonical identity	IP-3992
Responsibility	Controller/scheduler above licensed DDR5/MRDIMM-class PHY with QoS, telemetry and fault containment.
Delivery boundary	Soft IP / model
Evidence scope	RTL + models

Delivery and release binding

• Interface version and parameter set

• Clock/reset domains and integration constraints

• Companion memory, PHY and software requirements

• Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

The Bible records source/model or productization evidence for this IP. The selected HDL, verification and physical views are reviewed per release.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P1/P2 / SOURCE RTL BOUNDARY; DDR COMPLIANCE/PHY OPEN

Source basis: Bible v7.42 IP-3992

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

Contact: patrick@garmolabs.com | Product path: /ip/kenbe-ddr