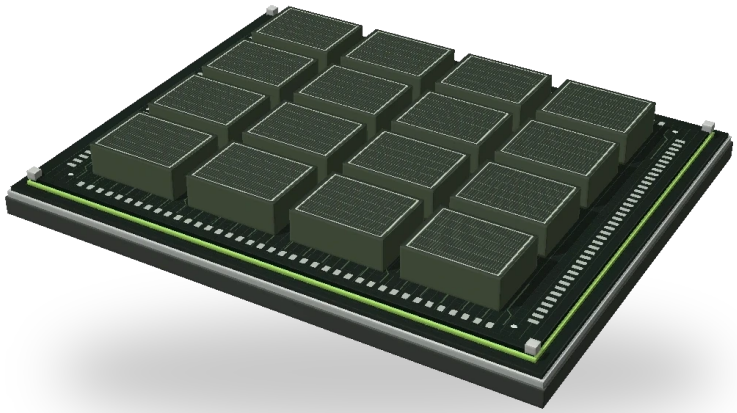
SPATIAL COMPUTING

MSR-X130

A heterogeneous spatial processor designed around the routing, memory and physical realities of mature-node silicon.



Architectural concept. Not a die photograph, physical layout or measured device.

IP-045 · Qualified release · Release-specific physical views

Function and architecture

- Fusion processing elements
- Sparse, solver, vector and floating-point mix
- Static transport, descriptors and local SRAM
- R1.0 package-ready implementation

Integration summary

Shared static transport and descriptor/DMA semantics let specialized engines cooperate under a route-aware architecture. Engine and derivative licensing are scoped independently.

Technical record

Canonical identity	IP-045
Responsibility	Flagship heterogeneous spatial superprocessor
Documented building blocks	Fusion processing elements; STF; descriptor/DMA; local SRAM; link; telemetry.
Delivery boundary	Release-specific physical views
Evidence scope	Qualified release

Delivery and release binding

- Exact SoC/top and configuration
- Clock, reset, power and pad contract
- Memory, PHY and package dependencies
- Release-specific PVT and signoff views

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

The later R1.0 record identifies MSR-X130 as signoff-complete and ChipIgnite package-ready, with controlled physical/signoff reports and release hashes.

The exact mature-node release does not establish advanced-node performance or returned-silicon proof.

Canonical status: Engineering build-spec family

Source basis: Bible v7.42 §§126–127, R1.0 controlled release ledger

Evaluation and licensing

Evaluation: Architecture and release evaluation. Production: Chip / SoC licensing program. Custom work: Custom silicon integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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