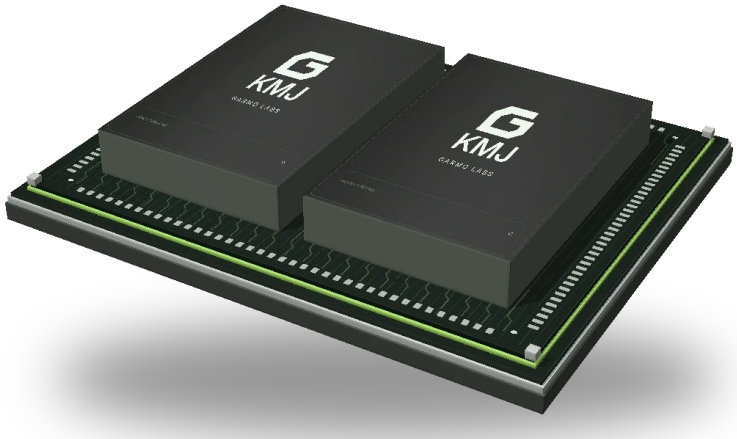
COHERENT COMPUTING

KMJ-X130

CPU, accelerator and memory execution connected through one coherent architecture for demanding mixed compute workloads.



Architectural concept. Not a die photograph, physical layout or measured device.

IP-062 · Qualified release · Release-specific physical views

Function and architecture

- Coherent CPU + accelerator architecture
- AI, HPC, graph and network composition
- Memory/fabric and RAS integration
- R1.0 package-ready implementation

Integration summary

Use the controlled S130 implementation as a proof and integration foundation. Larger chiplet or high-bandwidth-memory derivatives require their own physical qualification.

Technical record

Canonical identity	IP-062
Responsibility	Extreme-scale superchip
Documented building blocks	Full KMJ CPU/AI/HPC/memory/graph/network stack; chiplet fabric; HBM; RAS/security.
Delivery boundary	Release-specific physical views
Evidence scope	Qualified release

Delivery and release binding

- Exact SoC/top and configuration
- Clock, reset, power and pad contract
- Memory, PHY and package dependencies
- Release-specific PVT and signoff views

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

The later R1.0 record identifies KMJ-X130 as signoff-complete and ChipIgnite package-ready. Its controlled release is distinct from broader family roadmap configurations.

Package-ready is pre-silicon evidence, not foundry acceptance, returned devices or measured silicon characterization.

Canonical status: Engineering build-spec family

Source basis: Bible v7.42 §§126–127, R1.0 controlled release ledger

Evaluation and licensing

Evaluation: Architecture and release evaluation. Production: Chip / SoC licensing program. Custom work: Custom silicon integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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