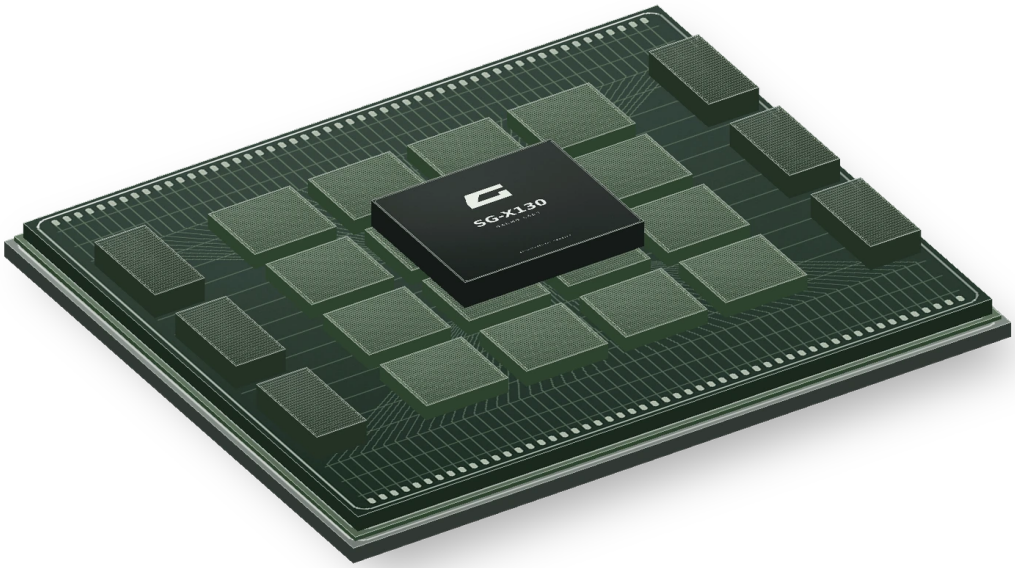
EXTREME-SCALE SG PROCESSOR

SG-X130

The extreme-scale SG architecture combines larger tile arrays, global connectivity, virtualization and reliability mechanisms.



Architectural concept. Not a die photograph, physical layout or measured device.

IP-070 · Architecture IP · Architecture

Function and architecture

- Large SG tile arrays
- many SGLink ports
- global fabric
- virtualization

Integration summary

Compose the selected SG tile-array configuration with its global fabric and SGLink ports. Preserve virtualization and fault-containment boundaries, and confirm memory, package/link and RAS contracts on the exact implementation rather than inheriting another SG variant’s results.

Technical record

Canonical identity	IP-070
Responsibility	Extreme-scale SG processor
Documented building blocks	Large SG tile arrays; many SGLink ports; global fabric; virtualization; RAS/self-healing.
Delivery boundary	Architecture
Evidence scope	Architecture IP

Delivery and release binding

- Exact SoC/top and configuration
- Clock, reset, power and pad contract
- Memory, PHY and package dependencies
- Release-specific PVT and signoff views

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Architecture and reusable technology are recorded in the controlled catalog. Request the exact release evidence for your intended integration.

Node-specific physical implementation and system qualification are scoped separately.

Canonical status: Engineering build-spec family

Source basis: Bible v7.42 IP-070

Evaluation and licensing

Evaluation: Architecture and release evaluation. Production: Chip / SoC licensing program. Custom work: Custom silicon integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

Contact: patrick@garmolabs.com | Product path: /silicon/sg-x130