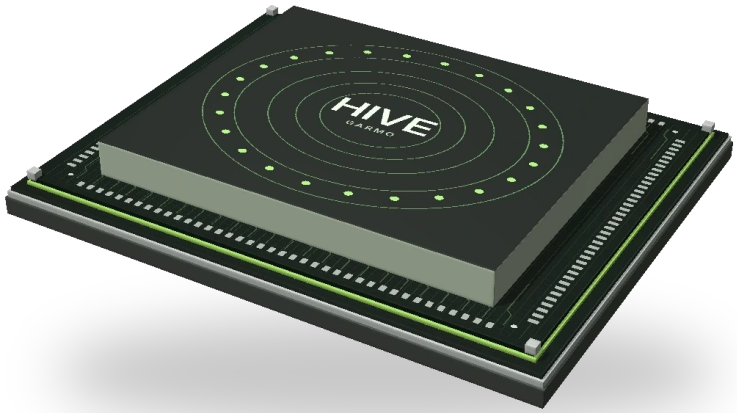
NEAR-FIELD SWARM CONNECTIVITY

NFESR-H4 HIVE

A near-field communication and swarm-coordination hub built around coherent field seeds, phase control and a shared digital integration fabric.



Architectural concept. Not a die photograph, physical layout or measured device.

IP-4708 · Source + model · RTL + reference models

Function and architecture

- Four electrostatic phase-modulation lanes
- Sixteen coherent field-seed banks
- 128-byte transmit and receive FIFOs
- Carrier-conflict avoidance, phase synchronization and host CSR

Integration summary

The HIVE SoC connects the common NFESR fabric to a dedicated chip top, with digital seed control, phase synchronization, receive voting, event/IRQ and Wishbone host access. Analog field drivers, receiver front ends, electrodes and package coupling are explicit external physical boundaries.

Technical record

Canonical identity	IP-4708
Responsibility	A near-field communication and swarm-coordination hub built around coherent field seeds, phase control and a shared digital integration fabric.
Delivery boundary	RTL + reference models
Evidence scope	Source + model

Delivery and release binding

- Exact SoC/top and configuration
- Clock, reset, power and pad contract
- Memory, PHY and package dependencies
- Release-specific PVT and signoff views

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Bible v7.42 §139 records the HIVE SoC as IP-4708 and binds the family to 117 reference, structural and artifact checks. HDL/CAD closure and mixed-signal physical qualification remained pending at the recorded cutoff.

The documented lane, seed-bank and FIFO counts are source-configuration parameters. Range, link rate, power, interference tolerance and field-coupling behavior require analog/package qualification and silicon measurement; no measured wireless performance is asserted.

Canonical status: SOURCE IMPLEMENTED / 117-TEST CAMPAIGN BOUND / HDL-CAD CLOSURE PENDING

Source basis: Bible v7.42 VERIFIED V29, §139.3–139.9; IP-4708 nfesr_hive_soc; pages 1222–1226

Evaluation and licensing

Evaluation: Architecture and release evaluation. Production: Chip / SoC licensing program. Custom work: Custom silicon integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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